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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/960,728	09/24/2001	Dominic Hugo Symes	550-258	4210

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EXAMINER	
HUISMAN, DAVID J	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 08/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/960,728	SYMES, DOMINIC HUGO	
	Examiner	Art Unit	
	David J. Huisman	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 Mayl 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9 and 11-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,9 and 11-15* is/are rejected.

7)☒ Claim(s) *7 and 8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 March 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. *see attached* .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-9 and 11-15 have been examined.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: RCE as received on 5/31/2006.

Claim Rejections - 35 USC § 101

3. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

4. Claims 14-15 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. More specifically, claims 14 and 15 do not produce a tangible result. Applicant should add language directed to storing said output data word Rd at the end of each of these claims.

5. The examiner recommends the following amendments, which were agreed upon by the examiner and applicant. Regarding claims 14 and 15:

- At the end of paragraph (ii), replace "; and" with --;--.
- At the end of paragraph (iii), replace "Rd." with --Rd; and--
- After paragraph (iii), insert --(iv) storing said output data word Rd.--

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1, 3-6, 9, 11-12, and 14-15 are rejected under 35 U.S.C. 102(b) as being anticipated by Motorola, "MC88110 - Second Generation RISC Microprocessor User's Manual," 1991 (herein referred to as Motorola).

8. Referring to claim 1, Motorola has taught apparatus for processing data, said apparatus comprising:

(i) a shifting circuit. See page 5-11, Fig.5-5, and note that data is shifted in multiple directions. A shifting circuit would inherently exist to perform such shifting in response to the ppack instruction.

(ii) a bit portion selecting and combining circuit. From Fig.5-5, it can be seen that data from multiple input words is selected and combined. Again, a circuit exists to perform this function in response to the instruction.

(iii) an instruction decoder, responsive to an instruction to control said shifting circuit and said bit portion selecting and combining circuit for performing an operation upon a data word Rn and a data word Rm (it is inherent that an instruction decoder exists in order to decode instructions prior to execution. The decoder, in response to the ppack instruction (Fig.5-5), will control the system such that the disclosed operation of Fig.5-5 is performed. In addition, the ppack

instruction selects and combines data from multiple data words Rn (rS1) and Rm (rS2)), wherein said operation yields a value given by:

(a) selecting a first portion of bit length A of said data word Rn extending from one end of said data word Rn. See Fig.5-5 and note that a 48-bit portion of rS1 (Rn) is selected. This portion extends from one end of Rn.

(b) selecting a second portion of bit length B of said data word Rm subject to an arithmetic right shift by a right shift amount specified as a shift operand within said instruction, said right-shift amount being independent of said bit length A of said first portion. See Fig.5-5 and note that a portion G1 (the shaded portion) is selected and shifted to the right towards the least significant end of output rD. The shift amount is independent of bit length A and the shift amount is determined by the type of instruction. In this case, the .16 is the operand which specifies how much to shift the data (it specifies the type of instruction which in turn specifies how the operation is performed). Also, for purposes of examination, the examiner is interpreting "arithmetic right shift" as being a right shift of an arithmetic value.

(c) combining said first portion and said second portion to form respective different bit position portions of an output data word Rd. See Fig.5-5.

9. Referring to claim 3, Motorola has taught an apparatus as described in claim 1. Motorola has further taught that the first portion extends from a least significant bit end of said data word Rn. See Fig.5-5.

10. Referring to claim 4, Motorola has taught an apparatus as described in claim 1. Motorola has further taught that said shift operand can specify a number of bit-positions representing an

amount of arithmetic right shift to apply to said data word Rm. Again, see Fig.5-5 and the preceding paragraph and note that values may be truncated to different sizes based on the instruction. And, different sized truncated portions will be shifted different amounts. So, an instruction operand such as the ".16" in the instruction, will specify a number of places to shift.

11. Referring to claim 5, Motorola has taught an apparatus as described in claim 1. Motorola has further taught that said first portion and said second portion abut within said output data word Rd. See Fig.5-5, and note that the first portion and second portion (G1) abut in the output data word.

12. Referring to claim 6, Motorola has taught an apparatus as described in claim 5. Motorola has further taught that said output data word has a bit length of C and C=A+B. Looking at Fig.5-5. The output data word is interpreted as the data spanning from G1 to α0. In this case, the output word has a bit length of 56 where A has a bit length of 48 an dB has a bit length of 8.

13. Referring to claim 9, Motorola has taught an apparatus as described in claim 1. Motorola has further taught that B=16. See the paragraph preceding Fig.5-5. It is disclosed that values may be truncated to 16 bits (so G1 and B1 would be 16 bits). Hence B=16.

14. Referring to claim 11, Motorola has taught an apparatus as described in claim 1. Motorola has further taught that said instruction combines a data value pack operation with a shift operation. See Fig.5-5. Shifting and packing is performed.

15. Referring to claim 12, Motorola has taught an apparatus as described in claim 1. Motorola has further taught that said shifting circuit is upstream of said selecting and combining circuit in a data path of said apparatus. Fig.5-5 shows that portions are selected, and then shifted. So, the shifting is upstream (after) the selecting part.

16. Referring to claim 14, the method of claim 14 if performed by the apparatus of claim 1. Consequently, claim 14 is rejected for the same reasons set forth in the rejection of claim 1.

17. Referring to claim 15, method of claim 14 is performed by the computer program provided on a computer readable medium of claim 15. Consequently, claim 15 is rejected for the same reasons set forth in the rejection of claim 14. Furthermore, it should be realized that the ppack instruction of Motorola would be part of a program that can be executed. And, it would therefore be stored on a computer readable medium.

18. Claims 1-2, 4-5, 9, 11-12, and 14-15 are rejected under 35 U.S.C. 102(b) as being anticipated by Digital Equipment Corporation, "VAX11 780 Architecture Handbook," 1977 (herein referred to as DEC).

19. Referring to claim 1, DEC has taught apparatus for processing data, said apparatus comprising:

(i) a shifting circuit. See page 7-18, and note that for the EXTV instruction, data is shifted (note the arrows that indicate shifting). A shifting circuit would inherently exist to perform such shifting in response to the EXTV instruction.

(ii) a bit portion selecting and combining circuit. Looking at the EXTV figure, it can be seen that data is selected and combined. Again, a circuit exists to perform this function in response to the instruction.

(iii) an instruction decoder, responsive to an instruction to control said shifting circuit and said bit portion selecting and combining circuit for performing an operation upon a data word Rn and a data word Rm (it is inherent that an instruction decoder exists in order to decode instructions

prior to execution. The decoder, in response to the EXTV instruction (page 7-18), will control the system such that the disclosed EXTV operation is performed. In addition, the EXTV instruction selects and combines data from multiple data words Rn and Rm), wherein said operation yields a value given by:

(a) selecting a first portion of bit length A of said data word Rn extending from one end of said data word Rn. See the EXTV figure and note that a first portion (the sign field) is selected. This portion extends from one end of Rn (notice the hatching).

(b) selecting a second portion of bit length B of said data word Rm subject to an arithmetic right shift by a right shift amount specified as a shift operand within said instruction, said right-shift amount being independent of said bit length A of said first portion. See the EXTV figure and note that a portion following the sign field (second word Rm) is selected and shifted to the right towards the least significant end of the output. The shift amount is independent of bit length A and the shift amount is indicated by the pos.rl operand in the instruction. The pos.rl field indicates how many bits to the right the second portion must be shifted right. For purposes of examination, the examiner is interpreting "arithmetic right shift" as being a right shift of an arithmetic value.

(c) combining said first portion and said second portion to form respective different bit position portions of an output data word Rd. See the output of the EXTV instruction on page 7-18.

20. Referring to claim 2, DEC has taught an apparatus as described in claim 1. DEC has further taught that said first portion extends from a most significant bit end of said data word Rn.

The sign field extends from the most significant portion of Rn because if you start at the most significant portion and travel right, you eventually encounter the sign field.

21. Referring to claim 4, DEC has taught an apparatus as described in claim 1. DEC has further taught that said shift operand can specify a number of bit-positions representing an amount of arithmetic right shift to apply to said data word Rm. Again, see the EXTV instruction and see the example of page 7-19. In the example, the pos.rl field is set to #5. This means that the portion will be shifted right 5 bits.

22. Referring to claim 5, DEC has taught an apparatus as described in claim 1. DEC has further taught that said first portion and said second portion abut within said output data word Rd. See the output of the EXTV instruction. Sign data (the first portion) and the second portion abut in the output.

23. Referring to claim 9, DEC has taught an apparatus as described in claim 1. DEC has further taught that B=16. Note that the size.rb operand specifies the size of the second portion. Clearly, the portion may be a size that is a subset of the overall input. Examples on page 7-19 show second portions of 10 bits, but portions of 1-31 may also be selected (note that a size of 32 causes a fault - see notes on page 7-19). Hence B=16.

24. Referring to claim 11, DEC has taught an apparatus as described in claim 1. DEC has further taught that said instruction combines a data value pack operation with a shift operation. See EXTV. Shifting and packing is performed.

25. Referring to claim 12, DEC has taught an apparatus as described in claim 1. DEC has further taught that said shifting circuit is upstream of said selecting and combining circuit in a

data path of said apparatus. EXTV shows that portions are selected, and then shifted. So, the shifting is upstream (after) the selecting part.

26. Referring to claim 14, the method of claim 14 if performed by the apparatus of claim 1. Consequently, claim 14 is rejected for the same reasons set forth in the rejection of claim 1.

27. Referring to claim 15, method of claim 14 is performed by the computer program provided on a computer readable medium of claim 15. Consequently, claim 15 is rejected for the same reasons set forth in the rejection of claim 14. Furthermore, it should be realized that the EXTV instruction of DEC would be part of a program that can be executed. And, it would therefore be stored on a computer readable medium.

Claim Rejections - 35 USC § 103

28. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

29. Claims 2 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Motorola.

30. Referring to claim 2, Motorola has taught an apparatus as described in claim 1. Motorola has further taught that the first portion extends from a least significant bit end of said data word Rn (see Fig.5-5) but not from a most significant bit end as claimed. However, as shown in In re Japikse 86 USPQ 70 (CCPA 1950), shifting locations of parts is generally not given patentable weight or would have been an obvious improvement. Specifically, looking at register rS1 if

Fig.5-5, each field holds a different value. These values could be stored in any order in the register or start at the most significant end. As long as the system knows which field is which, it makes no difference where they are located. Consequently, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Motorola such that the first portion extends from the most significant end instead of the least significant end.

31. Referring to claim 13, Motorola has taught an apparatus as described in claim 12. Motorola has not taught that said selecting and combining circuit is disposed in parallel to an arithmetic circuit within said data path. However, Official Notice is taken that having multiple operation units in parallel is well known and accepted in the art. When units are disposed in parallel, the processor may send multiple instructions to those units at the same time (i.e., more instructions may be executed at once). This increases parallelism, which in turn increases throughput. As a result, it would have been obvious to one of ordinary skill in the art at the time of the invention to have the selecting and combining circuit disposed in parallel with an arithmetic unit.

32. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over DEC.

33. Referring to claim 13, DEC has taught an apparatus as described in claim 12. DEC has not taught that said selecting and combining circuit is disposed in parallel to an arithmetic circuit within said data path. However, Official Notice is taken that having multiple operation units in parallel is well known and accepted in the art. When units are disposed in parallel, the processor may send multiple instructions to those units at the same time (i.e., more instructions may be executed at once). This increases parallelism, which in turn increases throughput. As a result, it

would have been obvious to one of ordinary skill in the art at the time of the invention to have the selecting and combining circuit disposed in parallel with an arithmetic unit.

Allowable Subject Matter

34. Claims 7-8 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David J. Huisman whose telephone number is (571) 272-4168. The examiner can normally be reached on Monday-Friday (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

DJH
David J. Huisman
August 19, 2006

RICHARD L. ELLIS
PRIMARY EXAMINER